

Mayank Agarwal

CONTACT INFORMATION	1006 W. Stoughton St #23 Urbana, IL-61801 USA	<i>Ph (Res):</i> 217-419-4989 (<i>Off:</i>) 217-333-4419 <i>E-mail:</i> magarwa2@uiuc.edu <i>WWW:</i> http://users.crhc.illinois.edu/~magarwa2/
OBJECTIVE	A full-time position in a research or development group.	
INTERESTS	Computer architecture and microarchitecture, parallel computing, compilers, operating systems, reliable computing.	
EDUCATION	University of Illinois at Urbana-Champaign August 2004 – Present <ul style="list-style-type: none">• PhD Student in Computer Science• GPA 3.90/4.0 after 9 semesters• Expected graduation date - March 2009• Title: “Quantifying, Extracting and Enhancing Implicit Parallelism in Applications” University of Illinois at Urbana-Champaign August 2004 – December 2006 <ul style="list-style-type: none">• M.S. in Computer Science Indian Institute of Technology Delhi July 2000 – May 2004 <ul style="list-style-type: none">• Bachelor of Technology in Computer Science and Engineering• GPA 9.1/10, Department Rank 2/45	
RESEARCH EXPERIENCE	Research Assistant, Implicitly Parallel Architectures (IPA) Group, UIUC (August, 2006 - Present) <p>I have been working on the PolyFlow project, with the objective of automatic under-the-covers (implicit) parallelization of single-threaded applications on multi-core architectures. My focus has been on the policy for partitioning applications into threads that maximizes the extracted parallelism. I have also been exploring bottleneck analysis and program transformations to enhance parallelizability of applications in this system. (Mentor: Prof. Matthew Frank)</p>	
INDUSTRIAL EXPERIENCE	Intern, Intel Research, Santa Clara, CA (Summer 2007) <p>I interned at the Architecture Research Lab (ARL) at Intel Santa Clara, California. I worked on architectural techniques that benefit the emerging Recognition, Mining and Synthesis (RMS) workloads. My focus was on novel data prefetching techniques, and support for scatter-gather operations on SIMD architectures.</p> Intern, nVIDIA Corporation, Santa Clara, CA (Summer 2005) <p>I interned at the Architecture Group at nVIDIA, Santa Clara, where I worked on the display unit of an ongoing GPU project. I also worked in the design and development of an SLI simulator, that allows linking of multiple GPUs to produce a single output.</p> Intern, Advanced Technology Center, TCS, Hyderabad, India (Summer 2003) <p>I developed security solutions for web services using SOAP (an XML-based protocol).</p>	
TEACHING EXPERIENCE	Teaching Assistant, Computer Systems Organization (CS433) (Fall 2005 and Spring 2006) <p>I served as the TA for CS433 (combined graduate and under-graduate course) under Prof. Sarita Adve. As part of my duties, I designed homeworks and examinations, took office hours, graded answer sheets, and taught some lectures.</p>	
SOME RELEVANT COURSES	Dynamic Translation and Optimization Reliable and Robust Software Systems Compiler Construction	Storage Systems Parallel Architectures Algorithms Computer Architecture Bio-Informatics Digital IC Design
SERVICE	Reviewer for ISCA, PLDI, HPCA, DSN.	

REFEREED
PUBLICATIONS

Mayank Agarwal; Matthew I. Frank; *"Re-Evaluating the Potential of Speculative Parallelization"*, Submitted for review to International Symposium on Computer Architecture, (ISCA-36).

Mayank Agarwal; Nitin Navale; Kshitiz Malik; Matthew I. Frank; *"Fetch-Criticality Reduction Through Control Independence"*, International Symposium on Computer Architecture, (ISCA-35), June, 2008.

Mayank Agarwal, Kshitiz Malik, Kevin M. Woley, Sam S. Stone and Matthew I. Frank, *"Exploiting Postdominance for Speculative Parallelization"*, International Symposium on High-Performance Computer Architecture (HPCA-13), February, 2007.

Kshitiz Malik; Mayank Agarwal; Sam S. Stone; Kevin M. Woley; Matthew I. Frank; *"Branch-mispredict Level Parallelism (BLP) for Control Independence"*, International Symposium on High-Performance Computer Architecture, (HPCA-14), February, 2008.

Kshitiz Malik; Mayank Agarwal; Vikram Dhar; Matthew I. Frank; *"PaCo: Probability-based Path Confidence Prediction"*, International Symposium on High-Performance Computer Architecture, (HPCA-14), February, 2008.

Kshitiz Malik; Mayank Agarwal; Matthew I. Frank; *"Adaptive Memory Synchronization (AMS): Balancing the Risks and Benefits of Inter-thread Load Speculation"*, Second Annual Reconfigurable and Adaptive Architecture Workshop (RAAW-2), held in conjunction with MICRO-40, December, 2007.

Ankit Mathur, Mayank Agarwal, Soumyadeb Mitra, Anup Gangwar, M. Balakrishnan, Subhashis Banerjee, *"SMPS: an FPGA-based prototyping environment for multiprocessor embedded systems"*, Thirteenth ACM/SIGDA Intl. Symposium on Field-Programmable Gate Arrays (FPGA-2005). (Poster)

NON-REFEREED
PUBLICATIONS

Mayank Agarwal, *"Exploiting Postdominance for Speculative Parallelization"*, Masters Thesis, Department of Computer Science, University of Illinois at Urbana-Champaign, December 2006.

Mayank Agarwal, Ankit Mathur, *"RtKer-MP: A Real-time Kernel for Multiprocessor Leon and Framework for Generating Application Specific Schedulers"*, Bachelors Thesis, Department of Computer Science and Engg, Indian Institute of Technology Delhi (IIT-Delhi), India, May 2004.

Sam S. Stone, Kevin M. Woley, Kshitiz Malik, Mayank Agarwal, Vikram Dhar and Matthew I. Frank, *"Synchronizing Store Sets (SSS): Balancing the Benefits and Risks of Inter-thread Load Speculation"*, University of Illinois Center for Reliable and High-Performance Computing Technical Report UILU-ENG-06-2221, Nov 17, 2006.

Kshitiz Malik, Kevin M. Woley, Samuel S. Stone, Mayank Agarwal, Vikram Dhar, Matthew I. Frank, *"Confidence Based Out-of-Order Renaming for Speculatively Multithreaded Processors"*, Univ. of Illinois Center for Reliable and High-Perf. Computing Tech. Report UILU-ENG-06-2208, June, 9, 2006.

AWARDS AND
ACHIEVEMENTS

Outstanding Teaching Assistant award for CS433 (Spring 2006).

Suresh Chandra Memorial Trust Award (Computer Science and Engg.) for the best software project at the 35th Convocation – 2004 at IIT Delhi.

Bachelors Thesis Project awarded third prize in Intel India Student Research Contest 2003-04.

One of the two Indian students selected for the International Lucent Global Science Scholars Award 2000-01 based on academic record and extra-curricular achievements.

Selected for the Kundan Lal Trust Scholarship Award 2000-01 for academic excellence, awarded to one student out of the whole first year batch at IIT-Delhi.

All-India rank of 14 in the IIT-JEE 2000 Joint Entrance Examination out of over 150,000 candidates.

Gold Medal for being among the top 30 students at the Indian National Physics Olympiad 2000

Among the top 20 students in India at the All India CBSE National Mathematics Olympiad 1999

COMPUTER SKILLS

Operating Systems: Linux (with kernel level programming), Windows

Programming Languages: C, C++, Java

Architectures: x86, MIPS, SPARC

Scripting: Shell scripting including Sed and Awk, Perl

STATUS

Citizen of India, in the United States of America on F-1 student visa.