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Ph.D. Student in Computer Science

Computer Architecture, Compilers

EXPERIENCE

Research Assistant	5/2003 - Present	CRHC	Urbana, IL	The Advanced Computing Systems group conducts research on computer architecture at the Center for Reliable and High-Performance Computing. Projects pursued included hardware-based dynamic optimization, soft error tolerance, runtime systems, and compiler-based multithreading. Current projects include massively parallel and accelerator architectures.
Architecture Intern	5/2005 - 9/2005	Intel Corp	Hillsboro, OR	Worked in performance team at Intel's Oregon site. Developed algorithms to improve the performance of video decoding, in particular more efficient ways to do binary arithmetic coding. Also evaluated performance of proposed instruction set extension for text processing.
Architecture Intern	5/2004 - 8/2004	NVIDIA Corp	Santa Clara, CA	Worked on graphics chip front-end architecture. Developed a compiler to process high-level description of graphics processor interface. The compiler uses this description to automatically generate a hardware description of components in the processor front-end.
Undergraduate Research Assistant	9/2001 - 4/2002	OceanStore	Berkeley, CA	The OceanStore group does research on distributed, long-term data storage. I wrote code for sending messages between several concurrent processes running over a network. I also wrote benchmarks for analyzing the performance of this and other portions of the OceanStore code base.
Hardware Verification Intern	5/2001 - 8/2001	Procket Networks	Milpitas, CA	Debugged and tested RTL designs for networking chips. Specific work included building verification environments, writing behavioral verification models, designing test suites, and designing randomized tests.
Undergraduate Research Assistant	6/2000 - 12/2000	UC Berkeley Multimedia Research Center	Berkeley, CA	At BMRC I worked on the MASH project, which is a toolkit for sending streaming multimedia over the Internet. I rewrote a decoder for streaming video to use MMX instructions, specifically rewriting the inverse DCT code and the colorspace conversion code in assembly language to use the specialized instructions.
Electrical leader	11/1998 - 4/2002	UC Berkeley Solar Car	Berkeley, CA	Technical activity 15hrs/week: Worked on car electrical systems, including motor control, solar array, and batteries. Experience with power electronics, including rectifiers, inverters, voltage regulation.

PUBLICATIONS

- Aqeel Mahesri, Daniel R. Johnson, Neal Crago, Sanjay J. Patel, **Tradeoffs in Designing Accelerator Architectures for Visual Computing**, to appear at the 41st International Symposium on Microarchitecture, November 2008.
- Omid Azizi, Aqeel Mahesri, Sanjay J. Patel, Mark Horowitz, **Area-Efficiency in CMP Core Design: Co-Optimization of Microarchitecture and Physical Design**, Workshop on Design, Architecture, and Simulation of Chip Multiprocessors (dasCMP), 41st International Symposium on Microarchitecture, November 2008.
- John H. Kelm, Daniel R. Johnson, Aqeel Mahesri, Steven S. Lumetta, Matthew Frank, Sanjay J. Patel, **SChISM: Scalable Cache Incoherent Shared Memory**, University of Illinois Technical Report, UILU-ENG-08-2212, August 2008.
- Wen-mei Hwu, Shane Ryoo, Sain-Zee Ueng, John H. Kelm, Isaac Gelado, Sam S. Stone, Robert E. Kidd, Sara S. Baghsorkhi, Aqeel A. Mahesri, Stephanie C. Tsao, Nacho Navarro, Steve S. Lumetta, Matthew I. Frank, and Sanjay J. Patel, **Implicit Parallel Programming Models for Thousand-Core Microprocessors**, Proceedings of the 44th Annual Design Automation Conference, June 2007.
- Nicholas J. Wang, Aqeel Mahesri, and Sanjay J. Patel, **Examining ACE Analysis Reliability Estimates Using Fault Injection**, 34th International Symposium on Computer Architecture, June 2007.
- Aqeel Mahesri, Nicholas J. Wang, Sanjay J. Patel, **Hardware Support for Software Controlled Multithreading**, Workshop on Design, Architecture, and Simulation of Chip Multiprocessors, 39th International Symposium on Microarchitecture, December 2006.
- Aqeel Mahesri and Sanjay Patel, **Exploiting Parallelism Between Control and Data Computation**, University of Illinois Technical Report, UILU-ENG-05-2214, September 2005.
- Aqeel Mahesri and Vibhore Vardhan, **Power Consumption Breakdown on a Modern Laptop**, Workshop on Power Aware Computing Systems, 37th International Symposium on Microarchitecture, December 2004
- Brian Fahs, Aqeel Mahesri, Francesco Spadini, Sanjay J. Patel, and Steven S. Lumetta, **The Performance Potential of Trace-based Dynamic Optimization**, University of Illinois Technical Report, UILU-ENG-04-2208, November 2004.
- Aqeel Mahesri, **Exploiting Control/Data Parallelism**, M.S. thesis, May 2004.
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EDUCATION**University of Illinois
Urbana-Champaign***Graduate Courses*
Computer ScienceElectrical and Computer
Engineering*Major Class Projects*
Advanced CompilersDynamic Optimization
Operating Systems
Physical VLSI Design
IC Fabrication**University of California
Berkeley***Undergraduate Courses*
Computer ScienceElectrical Engineering
Math and Science

Other

Major Class Projects
CompilersOperating Systems
Computer ArchitectureGraphics
Digital ICs**Pursuing Ph.D. in Computer Science**
Completed M.S. in Computer Science
May 2004Parallel Computer Architecture, Randomized Algorithms, Advanced Compilers, Dynamic Optimization, Networking, Advanced Operating Systems
Advanced Computer Architecture, Network Systems Modeling, Physical VLSI Design, Multithreaded Computer Architecture, IC Fabrication

Implemented a fast algorithm for copy coalescing and register allocation using SSA form, for the LLVM compiler infrastructure.

Developing a profile-based system for improving branch prediction accuracy.

Measured breakdown of laptop power consumption by component.

Wrote a tool for automatic placement and routing.

Fabricated a test wafer in instructional lab.

B.S. in Electrical Engineering and Computer Science Honors Program

May 2002

GPA 3.92

Data Structures, Machine Structures, Computer Architecture, Operating Systems, Algorithms, Computability and Complexity, Graphics

Signals and Systems, Circuits, Microelectronics, Digital ICs, Digital Logic Design

Calculus, linear algebra, differential equations, statistics, abstract algebra,

Galois theory, three semesters physics

Micro- and macroeconomic theory, comparative politics, city planning, cultural psychology, technical writing

Implemented a complete compiler for an object-oriented programming language (COOL), including scanning, parsing, semantic analysis, basic optimizations, and code generation.

Implemented OS kernel elements including multithreading, virtual memory, and network support.

Designed pipelined MIPS processor (using VHDL and Xilinx tools). Design included deep (7-stage) pipelining, branch prediction, and hierarchical memory system.

Developed physics-based simulation of human hair. Project was awarded class prize for originality.

Designed and did layout for 32-bit fast carry adder. Extensive use of CAD tools, including Magic and SPICE.

SKILLS

Skill Name	Skill Level	Last Used	Experience
Java	Intermediate	4 year ago	4 years
C	Expert	Currently used	10 years
C++	Expert	Currently used	9 years
MIPS, x86 Assembly	Expert	Currently used	4 years
Perl	Expert	Currently used	6 years
Verilog, VHDL	Intermediate	Currently used	2 years
SPICE	Intermediate	5 years ago	2 years
XML/XSLT	Intermediate	3 years ago	1 year