

Carry in	Carry out	Output
0	0	00
0	1	01
1	0	10
1	1	11

Outcome depends on relative delays of paths I and II,

① if path I is slower than II,
S input to slave latch stays 0,
and y_2 does not change

② if path II is slower,
output of and gate B
may become 1 for a short time
setting $y_2 = 1$. \Rightarrow incorrect
outcome

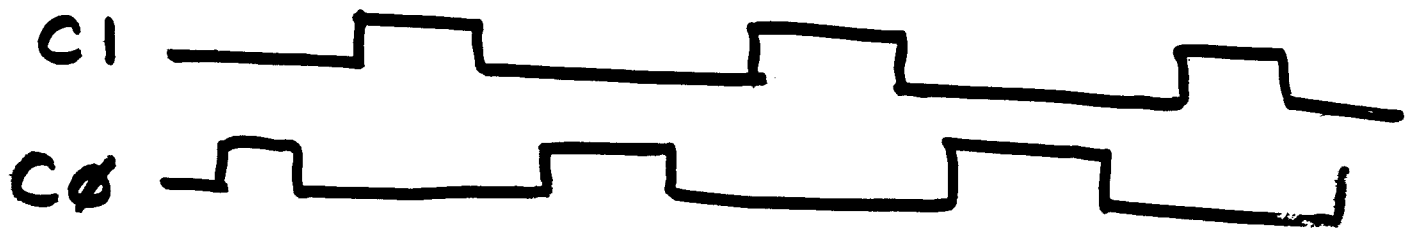
②

Essential hazard :

- Cannot be eliminated without controlling delays in the circuit
- present only in sequential circuits
- Occurs due to a signal that travels through two paths
 - one having only combinational ~~to~~ logic
 - one passing through a latch (or a memory element)

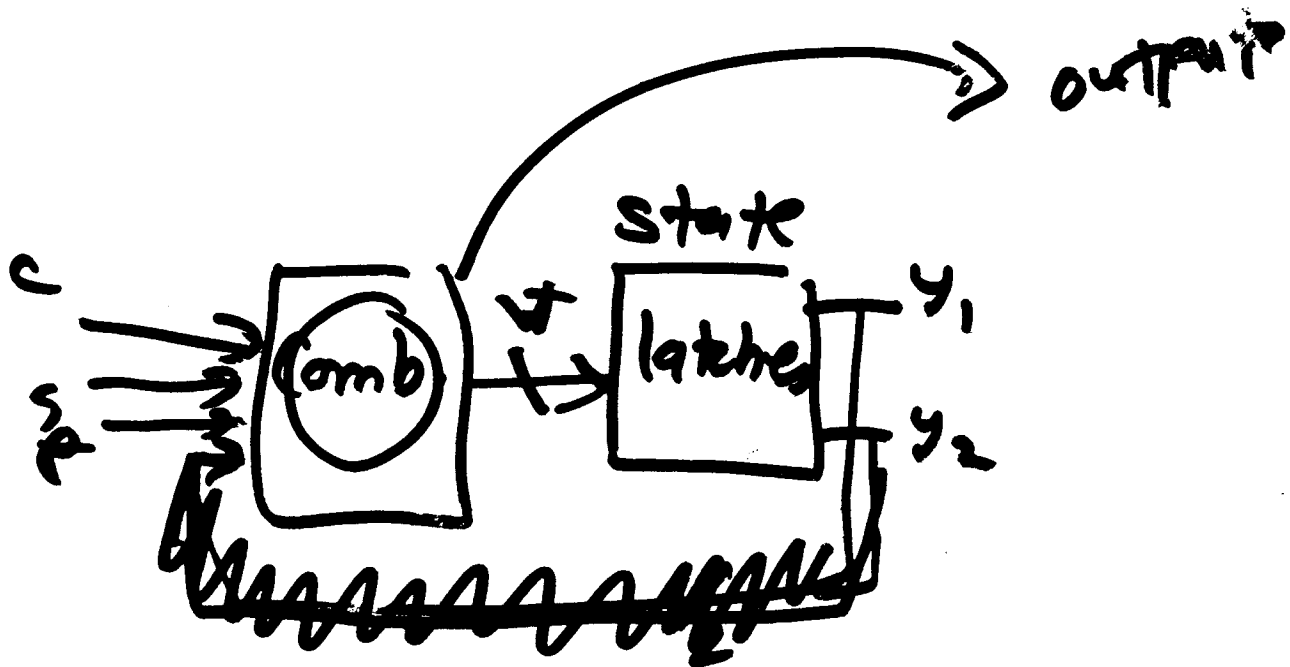
§ 7.8-1 Techniques for controlling essential hazards

- ⊛ delay path through a memory element (path 2) so that other path (path I) reflects input change earlier
 - alternatively, design path I to be always faster
- ⊛ Use non-overlapping two phase clock



The two ~~phase~~ phases are never high simultaneously

Use c_1 for master, and
 c_0 for slave

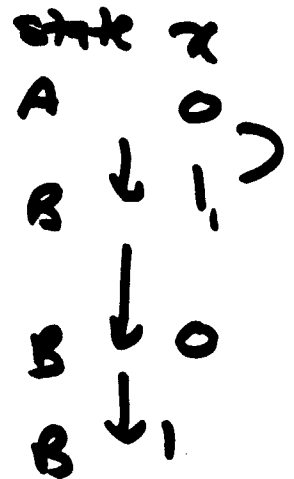
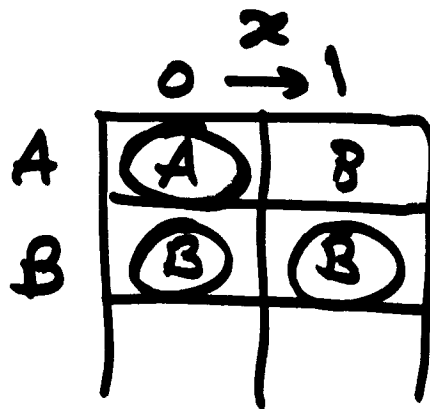
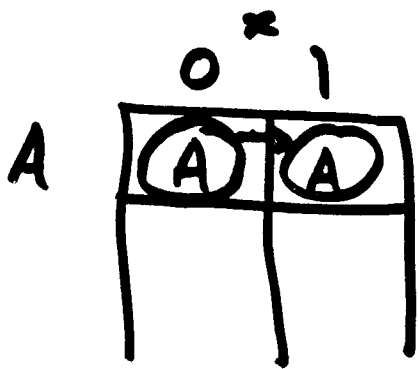


(5)

Detection of essential hazards

A total state represents an essential hazard if the state reached after one input change is distinct from that reached after 3 input changes.

Possible responses to single-input change:



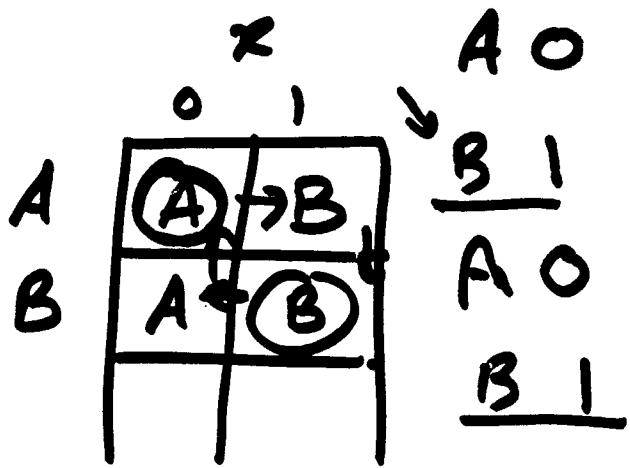
Initial total state: A, z=0

(a)

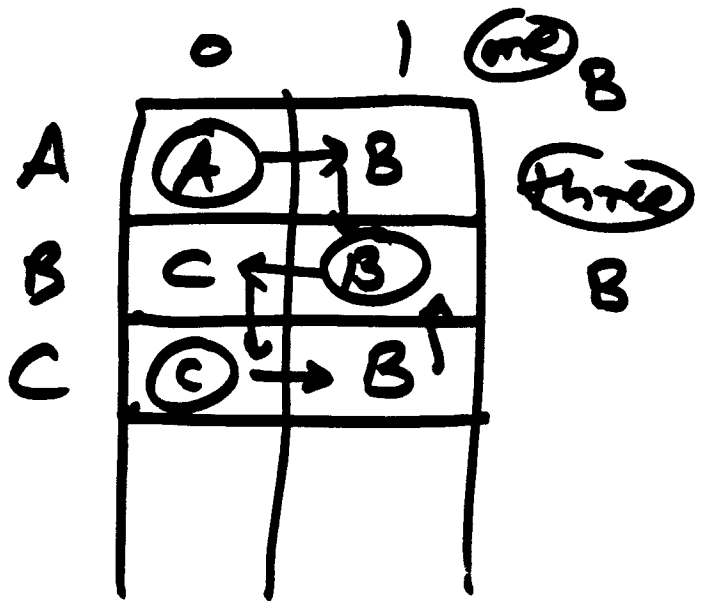
(b)

no essential hazard in (a), (b)

(c)

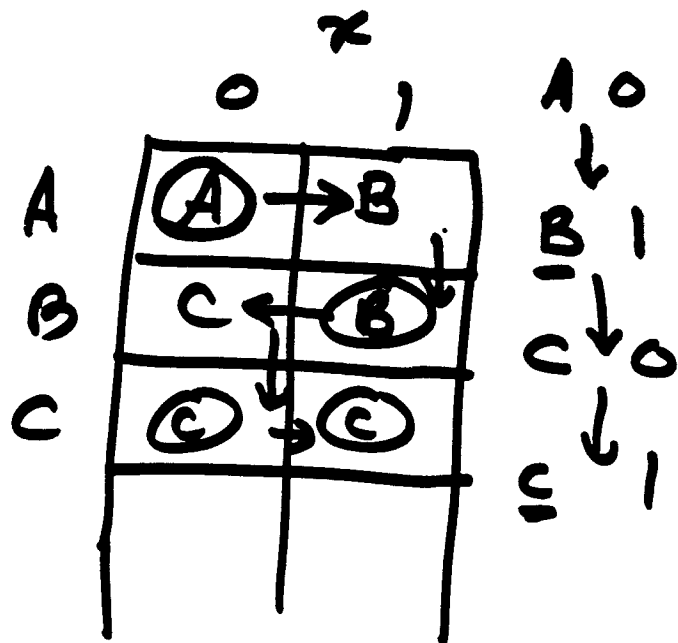


(c)

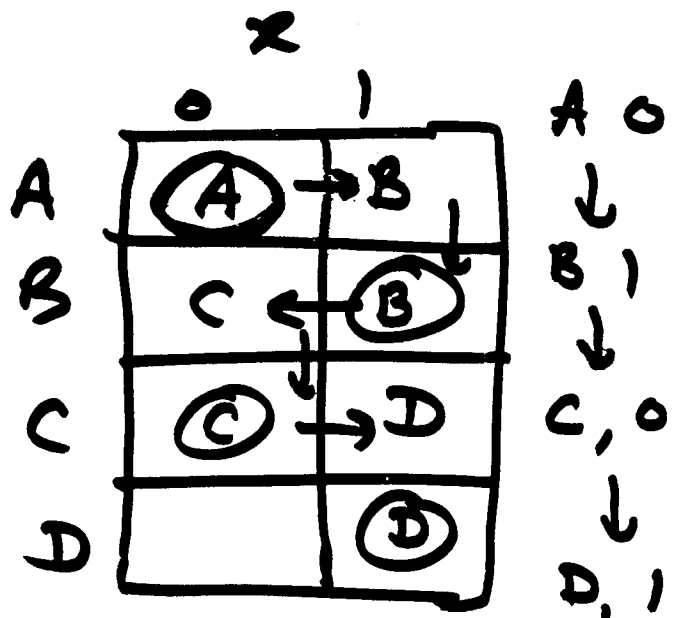


(d)

No essential hazard in (c), (d)



(e)



(f)

Essential hazard in

(e), (f)

7